AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A semiconductor device, comprising:

a die having

a first edge, and

a core;

a plurality of bond pads configured in ~~an~~ a staggered array between the first edge and the core, wherein the staggered array includes an inner ring and an outer ring of bond pads;

a first plurality of driver cells located between the first edge and the plurality of bond pads; and

a second plurality of driver cells located between the plurality of bond pads and the core.

2. (Cancelled)

3. (Currently Amended) The semiconductor device of claim ~~2~~1, further comprising a plurality of pre-drive cells located between the second plurality of driver cells and the core.

4. (Cancelled)

5. (Currently Amended) The semiconductor device of claim 1[[4]], further comprising a plurality of metal connections, each of the plurality of metal connections to couple one of the first and second pluralities of driver cells to one of the plurality of bond pads.

6. (Previously Presented) The semiconductor device of claim 5, further comprising a plurality of conductive interconnects, each of the plurality of pre-driver cells coupled to one of the first and second pluralities of driver cells by at least one of the plurality of conductive interconnects.

7. (Currently Amended) The semiconductor device of claim 6, wherein each of the plurality of conductive interconnects ~~substantially~~ are more narrow in width than each of the plurality of metal connections.

8. (Previously Presented) The semiconductor device of claim 7, wherein the first and second pluralities of driver cells each have a width of approximately 80 microns.

9-22. (Canceled)

23. (Previously Presented) The semiconductor device of claim 6, wherein each of the conductive interconnects coupling a pre-driver cell to one of the first and second driver cells has a width ranging from approximately 1-2 microns.

24. (Previously Presented) The semiconductor device of claim 6, wherein at least one pre-driver cell is coupled to one of the first and second driver cells via multiple conductive interconnects.

25. (Previously Presented) The semiconductor device of claim 6, wherein at least one conductive interconnect is disposed on a layer other than a layer where the bond pads are disposed.

26. (Previously Presented) The semiconductor device of claim 25, wherein at least one conductive interconnect is disposed on different layer underneath at least one bond pad.

27. (Previously Presented)The semiconductor device of claim 25, wherein at least one conductive interconnect is disposed on different layer underneath at least one driver cell.

28.-34. (Cancelled)

35. (New) A semiconductor device, comprising:

a die having

a first edge, and

a core;

a plurality of bond pads configured in an array between the first edge and the core;

a first plurality of driver cells located between the first edge and the plurality of bond pads;

a second plurality of driver cells located between the plurality of bond pads and the core; and

a plurality of conductive interconnects to couple each of the plurality of pre-driver cells to one of the first and second pluralities of driver cells, wherein at least one conductive interconnects is disposed on a layer other than a layer where the plurality of bond pads are disposed.

36. (New) The semiconductor device of claim 35, wherein the plurality of bond pads are configured in a staggered array.

37. (New) The semiconductor device of claim 36, further comprising a plurality of pre-drive cells located between the second plurality of driver cells and the core.

38. (New) The semiconductor device of claim 37, wherein the plurality of bond pads configured in the staggered array include an inner ring and an outer ring of bond pads.

39. (New) The semiconductor device of claim 38, further comprising a plurality of metal connections, each of the plurality of metal connections to couple one of the first and second pluralities of driver cells to one of the plurality of bond pads.

40. (New) The semiconductor device of claim 39, wherein each of the plurality of metal connections to couple one of the first and second driver cells to one of the bond pads has a width that is approximately up to 80 microns.

41. (New) The semiconductor device of claim 39, wherein each of the first driver cells is coupled to one of the outer ring of bond pads via one of the metal connections.

42. (New) The semiconductor device of claim 41, wherein each of the second driver cells is coupled to one of the inner ring of bond pads via one of the metal connections.

43. (New) The semiconductor device of claim 39, wherein at least one metal connection coupling a bond pad and a driver cell has a width equivalent to a width of one of the respective bond pad and the driver cell.

44. (New) A system comprising:

a lead frame;

a die coupled to the lead frame, the die having

a first edge, and

a core;

a plurality of bond pads configured in a staggered array between the first edge and the core, wherein the staggered array includes an inner ring and an outer ring of bond pads;

a first plurality of driver cells located between the first edge and the plurality of bond pads; and

a second plurality of driver cells located between the plurality of bond pads and the core.

45. (New) The system of claim 44, further comprising a plurality of pre-drive cells located between the second plurality of driver cells and the core.

46. (New) The system of claim 45, wherein at least one of the first and second driver cells is a ESD (electrostatic discharge) cell.

47. (New) The system of claim 46, wherein each of the driver cells provides at least one of a drive strength, reception of incoming signals, and ESD protection of the core.

48. (New) The system of claim 47, wherein each of the pre-drive cells provides communication between the core and one or more driver cells.